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CLEAN VERSION OF PENDING CLAIMS

METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT
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Claims 1-2, 4-14, 26-32 and 35-39, as of November 22, 2002 (Date of Response to First Office Action after RCE)

1.   (Amended) A method for reducing random single bit data loss in a FLASH memory circuit having a programming operation and an erase operation, comprising:

providing a semiconductor layer having a surface;

heating the layer in an atmosphere comprising a Hydrogen isotope wherein the Hydrogen isotope is incorporated into the layer; and

fabricating a memory circuit having a programming operation and an erase operation, comprising single bit data using the semiconductor layer, the fabricating comprising fabricating a gate region in the layer; treating a portion of the surface to form a thin layer of insulator film adjacent to the gate region and under the gate region; and heating the gate region and the thin layer in an atmosphere comprising Hydrogen isotope, wherein single bit data loss is reduced and wherein random single bit data loss is prevented in both the programming operation and the erase operation.

2.   The method of claim 1 and further comprising forming a film on the semiconductor layer that comprises the Hydrogen isotope.

4.   The method of claim 1 and further comprising exposing the semiconductor layer to a temperature that oxidizes the semiconductor layer.

5.   The method of claim 1 and further comprising exposing the semiconductor layer to a temperature that anneals the semiconductor layer.

6.   The method of claim 1 and further comprising exposing the semiconductor layer, sequentially, to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature.

7.   (Amended) The method of claim 1 and further comprising fabricating a second gate region within the memory circuit.

8.   The method of claim 7 and further comprising forming a film comprising Hydrogen isotope adjacent to the gate region of the memory circuit in order to reduce single bit data loss.

9.   The method of claim 7 and further comprising forming a film comprising Hydrogen isotope within the gate region of the memory circuit in order to reduce single bit data loss.

10.   The method of claim 1 and further comprising passivating the semiconductor layer in an atmosphere comprising Hydrogen isotope.

11.   The method of claim 1 and further comprising forming a field oxide in the semiconductor layer.

12.   The method of claim 11 and further comprising annealing the field oxide layer in an atmosphere that comprises Hydrogen isotope or a Hydrogen isotope containing compound.

13.   The method of claim 11 and further comprising annealing at a temperature that is at least about 800 degrees Centigrade.

14.   The method of claim 11 and further comprising oxidizing the annealed field oxide layer in an atmosphere that comprises Hydrogen isotope.

26. (Amended) A method of forming a non-volatile electrically alterable semiconductor FLASH memory cell having a programming operation and an erase operation, with reduced, random, single bit data loss in a memory circuit comprising:

providing a silicon substrate;

heating the silicon substrate in an atmosphere comprising a Hydrogen isotope wherein the Hydrogen isotope is incorporated into the silicon substrate;

fabricating a field oxide region and a channel region over or within the silicon substrate;

heating the silicon substrate with the field oxide region and channel region in an atmosphere comprising a Hydrogen isotope wherein the Hydrogen isotope is incorporated into the layer;

growing an oxide over the channel region in an atmosphere enriched in Hydrogen isotope;

fabricating at least one gate member; and

passivating the memory cell having a programming operation and an erase operation, comprising single bit data loss in an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss, wherein random single bit data loss is prevented in both the programming operation and the error operation.

27. The method of claim 26 and further including nitridizing the field oxide region by annealing in an atmosphere comprising Hydrogen isotope or a compound that comprises Hydrogen isotope.

28. The method of claim 26 and further comprising nitridizing at a temperature that is greater than or equal to about 800 degrees Centigrade.

29.   The method of claim 26 and further including oxidizing the nitridized field layer in an atmosphere that comprises Hydrogen isotope.

30.   The method of claim 26 and further comprising introducing the Hydrogen isotope by thermal oxidation.

31.   The method of claim 26 and further comprising introducing the Hydrogen isotope by pyrolytic diffusion of Hydrogen isotope into the memory cell.

32.   The method of claim 26 and further comprising introducing the Hydrogen isotope by RF sputter deposition.

35.   (Amended) A method for treating a non-volatile, electrically alterable semiconductor memory cell, thereby reducing random, single bit data loss in a memory circuit, comprising:

    providing a non-volatile, electrically alterable semiconductor memory cell comprising single bit data; and

    exposing the memory cell to an atmosphere that comprises Hydrogen isotope by sputter deposition or pyrolytic diffusion, thereby reducing single bit data loss.

36.   The method of claim 35 and further including heating the atmosphere.

37.   (Amended) A method for overlaying source and drain regions of a non-volatile, electrically alterable semiconductor memory cell having a programming operation and an erase operation, with a thermal oxide layer thereby reducing random, single bit data loss in a memory circuit, comprising:

    providing a silicon substrate and providing a memory cell, having a programming operation and an erase operation, the memory cell comprising single bit data;

defining source and drain regions in the silicon substrate and exposing the source and drain regions to an environment comprising Hydrogen isotope; and

growing the thermal oxide layer over the source and drain regions in an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss in the programming operation and the erase operation in the memory cell.

38. The method of claim 37 and further comprising heating the atmosphere that comprises Hydrogen isotope.

39. The method of claim 37 and further comprising defining the source and drain regions by targeted Hydrogen isotope implantation.